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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,030	07/30/2001	Michael John Erickson	10017840-1	1031

7590 09/01/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

CHU, GABRIEL L

ART UNIT	PAPER NUMBER
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2114

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/918,030	Applicant(s) ERICKSON ET AL.	
	Examiner Gabriel L. Chu	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-8 is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☒ Claim(s) 3 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6427198 to Berglund et al. in view of US 6691205 to Zilberman. Referring to claim 1, Berglund et al. disclose a method of updating programmable device configuration code stored in an EEPROM of a system, the system having separate management and system processors (From line 20 of column 1, "Devices that may be included in a computer system include a configuration processor that performs configuration and initialization operations during system initialization, one or more central processing units (CPUs), one or more riser cards having attached memory cards, such as dual in-line memory modules (DIMMs), and other components."), comprising executing a sequence for updating programmable device configuration code on a management processor of the system, the sequence for updating programmable device configuration code further comprising the steps of: erasing the EEPROM (Wherein altering an EEPROM entails electrically erasing the programmable read only memory).; writing at least one block of configuration code to the EEPROM (From line 52 of column 1, "In such case, before the system can function with the new configuration, the configuration processor code would

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have to be updated to reflect this new configuration. This complicates altering the system configuration because any change will have to be accompanied by a change to the configuration processor code by modifying the configuration memory, e.g., PROM, EEPROM.”). Although Berglund et al. do not specifically disclose checking for errors after writing the at least one block, the errors including failure of a FIFO to empty, and retrying the step of writing at least one block upon error, an error from a FIFO failing to empty and a subsequent retry is known in the art. An example of this is shown by Zilberman, from line 50 of column 3, “In the case where the data of a system's logical block N is written (FIG. 1) onto the flash media from memory buffer A, the data of logical block N+1 is being simultaneously received from the host interface to the memory buffer B. Here and in the following descriptions, the "logical block" stands for one or more host system transfer units (sectors). The size of the "logical block" is determined by the convenience and performance of the flash operations. For example in the case of AND or NAND-technology flash, it could be set to the page size of the used flash array. The stream of data transferred from the host is viewed by the storage system as a sequence of logical blocks N, N+1, N+2, etc. If there are only 2 logically independent memory buffers, upon completion of the data transfer into B, software should wait for the completion of the flash write operation from A and inspect the flash write status. If the write operation has failed, it can be retried at another place of the flash media. When the write operation is successful, memory buffer A can be considered empty and, two new simultaneous transfers can be initiated: block N+1 from the memory buffer B to the flash media and block N+2 from the host interface to the memory buffer A.” A person of

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ordinary skill in the art at the time of the invention would have been motivated to retry the write to flash from a non-empty buffer because, from line 65 of column 3 of Zilberman, "the write operation has failed". Further, although Berglund et al. and Zilberman do not specifically disclose said EEPROM may comprise EEPROMs, using multiple modules of memory to store data is notoriously well known in the art. An example of this is a memory bank comprising multiple memory units. A person of ordinary skill in the art at the time of the invention would have been motivated to use multiple memory units because it provides more storage space.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6427198 to Berglund et al. in view of US 6691205 to Zilberman as applied to claim 1 above, and further in view of US 5894571 to O'Connor. Although Berglund et al. in view of Zilberman do not specifically disclose the step of verifying that a file contains configuration code compatible with the system, having configuration code that is compatible with the system is known in the art. An example of this is shown by O'Connor, from line 50 of column 3, "It is advantageous that the disclosed method reduces technical support and warranty costs of the manufacturer. The software configuration written to CD-ROM is a verified combination of software components that is known to be compatible with the assembled hardware components. If a problem arises in subsequent operation of the computer system, the original software configuration can be restored simply and efficiently from the CD-ROM." A person of ordinary skill in the art at the time of the invention would have been motivated to verify configuration code compatibility because, from line 50 of column 3 of O'Connor, "It is

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advantageous that the disclosed method reduces technical support and warranty costs of the manufacturer.”

Allowable Subject Matter

4. Claims 4-8 are allowed.

5. The following is an examiner’s statement of reasons for allowance: Referring to claims 4-8, the prior art does not teach or fairly suggest verifying compatibility of the file with the serial bus, in the scope and context of claim 4.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Referring to claim 3, the prior art does not teach or fairly suggest, in light of the parent claim, the step of verifying that a file contains configuration code compatible with the system comprises polling a JTAG bus of the system to determine the configuration of the JTAG bus, and comparing the configuration with a configuration stored in the file.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 4914576 to Zelley et al.

US 5101490 to Getson, Jr. et al.

US 5343478 to James et al.

US 6044025 to Lawman

US 6255849 to Mohan

US 6501682 to Yoshida

US 6526332 to Sakamoto et al.

US 6614259 to Coutts-Martin et al.


US 6622206 to Kanamaru et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc


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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100